What Is Claimed Is:

1. A high clamping circuit ensuring that a voltage level at a node is below an upper limit, said high clamping circuit comprising:

a NMOS transistor drawing a substantial amount of current from said node when said voltage level at said node is greater than or equal to said upper limit.

2. The high clamping circuit of claim 1, further comprising a PMOS transistor which is turned on when said voltage level at said node is greater than or equal to said upper limit, wherein turning on of said PMOS transistor causes said NMOS transistor to draw said substantial amount of current.

3. A clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range.

4. The clamping circuit of claim 3, further comprising a biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range.

5. The clamping circuit of claim 4, wherein said first transistor and said current amplifier are contained in a high clamping circuit which clamps said voltage to said upper limit of said specified range, wherein said voltage level of said bias signal is determined by said upper limit,

wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and

said current amplifier is connected to both of said source terminal and said drain

terminal of said first transistor.

6. The clamping circuit of claim 4, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

7. The clamping circuit of claim 6, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

8. The clamping circuit of claim 4, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

9. The clamping circuit of claim 8, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

10. The clamping circuit of claim 4, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

11. The clamping circuit of claim 10, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

12. The clamping circuit of claim 4, wherein said first transistor and said current amplifier are contained in a low clamping circuit which clamps said voltage to said lower limit of said specified range, wherein said voltage level of said bias signal is determined by said lower limit, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

13. A device comprising:

a high clamping circuit ensuring that a voltage level at a node is below an upper limit, said high clamping circuit comprising a NMOS transistor drawing a substantial amount of current from said node when said voltage level at said node is greater than or equal to said upper limit.

14. The device of claim 13, further comprising a PMOS transistor which is turned on when said voltage level at said node is greater than or equal to said upper limit, wherein turning on of said PMOS transistor causes said NMOS transistor to draw said substantial amount of current.

15. A device comprising:

a clamping circuit ensuring that a voltage level at a node is within a specified range, said clamping circuit comprising:

a first transistor designed to be turned on when said voltage level is outside of said specified range; and

a current amplifier drawing a substantial amount of current from said node when said first transistor is turned on, which causes said voltage level at said node to be pulled to within said specified range.

16. The device of claim 15, wherein said clamping circuit further comprises a

biasing circuit generating a bias signal to a gate terminal of said first transistor, wherein a voltage level of said bias signal is determined by an upper limit or a lower limit of said specified range.

17. The device of claim 16, wherein said first transistor and said current amplifier are contained in a high clamping circuit which clamps said voltage to said upper limit of said specified range, wherein said voltage level of said bias signal is determined by said upper limit,

wherein said first transistor comprises a PMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and

said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

18. The device of claim 16, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to a drain terminal of said third transistor, a gate terminal of said third transistor receiving a third bias voltage, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to said source terminal of said first transistor.

19. The device of claim 18, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

20. The device of claim 16, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to each of a drain terminal and a gate terminal of said third transistor, a source terminal of each of said third transistor and said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor.

21. The device of claim 20, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

22. The device of claim 16, wherein said current amplifier comprises:

a third transistor and a fourth transistor, wherein a gate terminal of said fourth transistor is connected to both drain and gate terminals of said third transistor, a source terminal of said fourth transistor is connected to ground, said drain terminal of said third transistor is connected to a drain terminal of said first transistor, and a drain terminal of said fourth transistor is connected to a source terminal of said first transistor; and

a resistor connected between a source terminal of said third transistor and ground.

23. The device of claim 22, wherein each of said third transistor and said fourth transistor comprises a NMOS transistor.

24. The device of claim 16, wherein said first transistor and said current amplifier are contained in a low clamping circuit which clamps said voltage to said lower limit of said specified range, wherein said voltage level of said bias signal is determined by said lower limit, wherein said first transistor comprises a NMOS transistor, wherein a source terminal of said first transistor is connected to said node, a drain terminal of said first transistor is connected to said current amplifier, and said current amplifier is connected to both of said source terminal and said drain terminal of said first transistor.

25. The device of claim 24, wherein said device comprises a wireless base station, said device further comprising:

an antenna receiving an external signal; and

an analog processor processing said external signal.